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06ES32

Third Semester B.E. Degree Examination, January 2013
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the diode equivalent circuit with its characteristics. **(06 Marks)**

b. Explain transition and diffusion capacitance in an P-N junction diode. **(06 Marks)**

c. Plot the transfer characteristic for the circuit shown in Fig. Q1(c) and write the transfer characteristic equation. Sketch V_0 if $V_i = 40\sin\omega t$. Assume $V_K = 1$ V for the diode. **(08 Marks)**

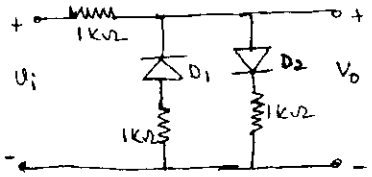

Fig. Q1 (c)

2 a. Define operating point. Explain its significance. **(04 Marks)**

b. Derive an expression for I_B, I_C and V_{CE} for an collector feedback bias. **(08 Marks)**

c. Design an emitter stabilized network shown in Fig. Q2(c) using the following data: **(08 Marks)**

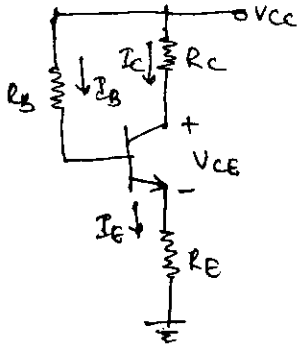

Fig. Q2 (c)

$I_{CQ} = \frac{1}{2} I_C(sat)$, $V_{CEQ} = \frac{1}{2} V_{CC}$

$V_{CC} = 20$ V, $I_C(sat) = 10$ mA

$\beta = 120$, $R_C = 4R_E$

Assume $I_E \cong I_C$

3 a. Derive an expression for Z_i, Z_o, A_v and A_I for common-emitter configuration using emitter bias with unbypassed R_E. (Using r_e model) **(10 Marks)**

b. For the fixed bias configuration shown in Fig. Q3(b), calculate

i) A_{VNL}, Z_i and Z_o

ii) A_V, A_{VS} and A_I

iii) Calculate V_o, if $V_S = 20$ mV. Take $\beta = 100$ **(10 Marks)**

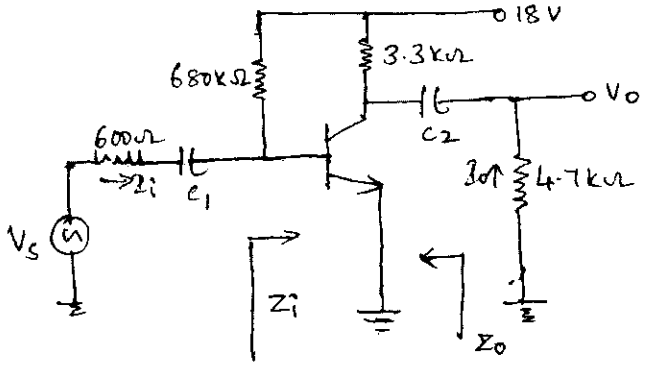

Fig. Q3 (b)

4 a. Derive an expression for Miller input capacitance and Miller output capacitance. **(10 Marks)**

b. For the circuit shown in Fig. Q4(b), calculate the following:

i) r_e, ii) Input existence R_i iii) Mid band voltage gains $A_V = \frac{V_0}{V_s}$ and $A_{VS} = \frac{V_0}{V_s}$

iv) lower cutoff frequency due to C_C. For transistor $\beta = 100$ and $r_0 = \infty$. **(10 Marks)**

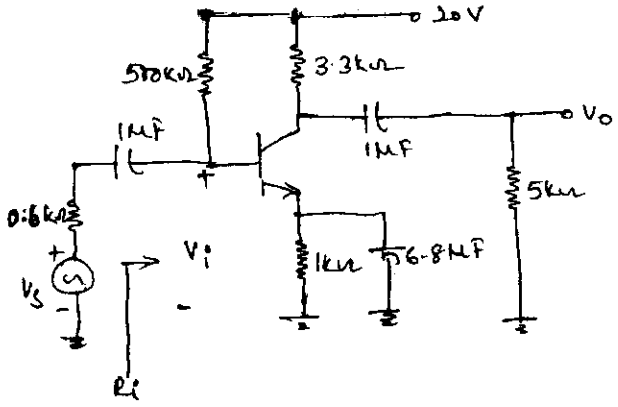

Fig. Q4 (b)

PART – B

5 a. Explain the difference between cascade and cascode connections and its application. **(05 Marks)**

b. Derive an expression for Z_i, Z_o, A_v for Darlington emitter follower. **(10 Marks)**

c. Explain feed back amplifier topologies. **(05 Marks)**

6 a. With a neat circuit diagram, explain transformer coupled class A amplifier and derive the expression for AC power delivered to the load, show maximum efficiency is 50%. **(10 Marks)**

b. The following readings are available for a power amplifier. Calculate the second harmonic distortion in each case:

i) $V_{CEQ} = 10$ V, $V_{CE(max)} = 18$ V, $V_{CE(min)} = 1$ V

ii) $V_{CEQ} = 10$ V, $V_{CE(max)} = 19$ V, $V_{CE(min)} = 1$ V **(05 Marks)**

c. For the circuit shown in Fig. Q6 (c) the input signal results in a peak base current of 1 mA

i) Calculate the ac output power.

ii) Calculate the dc input power dissipated by the circuit.

iii) Calculate the efficiency. **(05 Marks)**

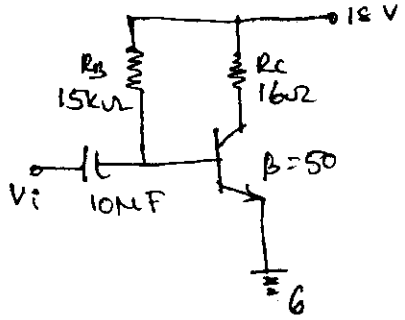

Fig. Q6 (c)

7 a. Explain the basic principle of oscillators. **(06 Marks)**

b. Explain with a neat circuit diagram the operation of R-C phase shift oscillator. **(08 Marks)**

c. A crystal has the following parameters:

L = 0.334 H, C = 0.065 pF, C_M = 1 pF, R = 5.5 kΩ

i) Calculate the series resonant frequency.

ii) Calculate the parallel resonant frequency.

iii) Find the Q of the crystal. **(06 Marks)**

8 a. Derive an expression for A_v, Z_i and Z_0 for an JFET source follower. **(10 Marks)**

b. For the network shown in Fig. Q8 (b), V_{GSQ} = -2.86 V, I_{DQ} = 4.56 mA, I_{DSS} = 16 mA, V_P = - 4V, Y_{OS} = 30 µs. Determine i) g_m ii) r_d iii) z_i and iv) z_0 without r_d and v) A_v without r_d. **(10 Marks)**

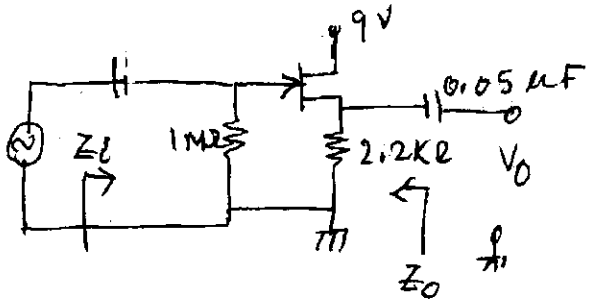

Fig. Q8 (b)

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